ABSTRACT OF THE DISCLOSURE

Formerly, in a microfabrication process of a semiconductor integrated circuit, there has been a problem of occurrence of a malfunction of a circuit during a scan test due to a skew resulting from factors, such as manufacturing variation and a delay calculation error, which have not been detected in simulation. In the present invention, for a plurality of flip-flop circuits which configure a scan chain, by arranging a clock circuit for scan which supplies a clock signal during the scan test separately from a clock circuit for normal operation which supplies a clock signal during a normal operation, arranging a lattice-shaped wiring portion for the clock circuit for scan, and supplying the clock signal for scan to each flip-flop circuit from the lattice-shaped wiring portion, generation of the clock skew resulting from the effect of the delay calculation error or the manufacturing variation in the microfabrication process is prevented, thereby preventing the malfunction during the scan test.